REMARKS

Summary Of Office Action

Claims 1-41 and 43-53 were pending in this application.

Claims 1-3, 9, 13-15, 21, 25, 26, 29, 31, 32, 38, 43-45 and 51 were rejected under 35 U.S.C. § 103(a) as being obvious from Stevens et al. U.S. Patent No. 6,226,729 (hereinafter "Stevens") in view of Hartwell U.S. Patent No. 6,724,850 (hereinafter "Hartwell").

Claims 4, 5, 7, 8, 10-12, 16, 17, 19, 20, 22-24, 27, 28, 30, 33, 34, 36, 37, 39-41, 46, 47, 49, 50, 52 and 53 were rejected under 35 U.S.C. § 103(a) as being obvious from Stevens and Hartwell in further view of Johnson et al. U.S. Patent No. 5,577,236 (hereinafter "Johnson").

Claims 6, 18, 35, and 48 were rejected under 35 U.S.C. § 103(a) as being obvious from Stevens and Hartwell in further view of Olarig et al. U.S. Patent No. 6,134,638 (hereinafter "Olarig").

Summary Of Applicant's Reply

Applicant has amended claims 1, 9, 11-13, 21, 23-26, 29-31, 38, 40, 41, 43, and 51-53 to more particularly define the invention. No new matter has been added and all of the amendments are fully supported by the original specification.

Reconsideration of this application in view of the amendments and the following remarks is respectfully requested.

Applicant's Reply to the 35 U.S.C. § 103(a) Rejections

Claims 1-3, 9, 13-15, 21, 25, 26, 29, 31, 32, 38, 43-45 and 51 were rejected under 35 U.S.C. § 103(a) as being obvious from Stevens in view of Hartwell. Claims 4, 5, 7, 8,

10-12, 16, 17, 19, 20, 22-24, 27, 28, 30, 33, 34, 36, 37, 39-41, 46, 47, 49, 50, 52 and 53 were rejected under 35 U.S.C. § 103(a) as being obvious from Stevens and Hartwell in further view of Johnson. Claims 6, 18, 35, and 48 were rejected under 35 U.S.C. § 103(a) as being obvious from Stevens and Hartwell in further view of Olarig. These rejections are respectfully traversed.

Amended independent claims 1, 9, 11-13, 21, 23-26, 29-31, 38, 40, 41, 43, and 51-53 are, at least in part, directed toward methods, memory controller, and apparatus for selecting an operating speed of a memory module interface. The number of memory modules is counted and a running tally of the number of memory modules is maintained based on the counting. Multiple clock signals are simultaneously generated at different frequencies to provide a selectable operating speed for the memory module interface. The maximum speed at which all of the memory module can operate is determined. Based on at least a final tally of the number of memory modules, only one of the multiple clock signals is selected to provide the operating speed of the memory module interface, where the operating speed is slower than the determined maximum speed. The selected clock signal is then provided to all of the memory modules.

The amendments to the independent claims further clarify the feature of applicant's claims argued in the previous Reply to Office Action, dated October 12, 2006. In particular, applicant's claims have been amended to specify that "a maximum speed at which all of the plurality of memory modules can operate [is determined]" and that an operating speed "slower than the determined maximum speed" is selected based at least on a final tally of the number of memory modules. In other words, an operating speed that is slower

than the maximum speed may be selected for the memory module interface based on the total number of memory modules. For example, if only two memory modules are present that can operate at a maximum speed of 100 MHz an operating speed of 100 MHz may be selected. However, when four of these 100 MHz memory modules are present, a slower operating speed such as 83 MHz may be selected. Support for this example may be found in applicant's specification, for example, on page 8, lines 3-16. In this example, increasing the number of memory modules may affect the speed at which all of the memory modules can operate. Applicant's claimed feature of selecting an operating speed based on a final tally of the number of memory modules enables the maximum speed to be used when there are only a few memory modules and a slower speed when there are more memory modules. Without this feature, the slower speed must always be used (i.e., the system will always operate at a slower speed that can support the maximum number of memory modules). Applicant respectfully submits that none of the references cited by the Examiner show or suggest this feature of applicant's independent claims.

The Examiner contends that Stevens shows selecting a clock signal "based on at least a final tally of the number of said memory modules." This, however, is not the case. Stevens only refers to selecting a clock frequency "at which all RIMMs may operate." Stevens, column 13, lines 44-45. Thus, while Stevens refers to querying each memory module within the system to determine the speeds at which each of the memory modules operate, the number of memory modules is not counted. In other words, while the clock signal ultimately selected by Stevens must be operable with all of the memory modules, only the speed of each of the memory modules is a factor the selection - not the number of memory modules. For

example, there is nothing in Stevens that shows or suggests selecting a faster clock signal when there are only two memory modules having the same speed (e.g., 100 MHz) or a slower clock signal where there are four or more memory modules also having that same speed (e.g., 100 MHz).

Thus, applicant respectfully submits that Stevens does not show or suggest selecting an operating speed "based on at least a final tally of the number of said memory modules," where the selected operating speed is "slower than the determined maximum operating speed," as specified by applicant's amended independent claims.

Furthermore, no combination of Stevens with any of Hartwell, Johnson, and Olarig makes up for this deficiency in Stevens. Therefore applicant respectfully submits that neither Stevens nor Johnson nor Olarig shows or suggests all of the elements of applicant's independent claims. Whether or not the combination of these references are proper, the combination of features which these references cumulatively contribute also falls short of showing or suggesting applicant's claimed

For at least the reasons discussed above with respect to independent claims 1, 9, 11-13, 21, 23-26, 29-31, 38, 40, 41, 43, and 51-53, dependent claims 2-8, 10, 14-20, 22, 27, 28, 32-37, 39, and 44-50, which depend directly or indirectly from claims 1, 9, 11-13, 21, 23-26, 29-31, 38, 40, 41, 43, and 51-53 are also not rendered obvious from the various combinations of Olarig, Ikeda, Schwartz, Johnson, Chang, Stevens and Hartwell (i.e., dependent claims are patentable if their independent claim is patentable).

Accordingly, applicant respectfully requests that the rejections of dependent claims 2-8, 10, 14-20, 22, 27, 28, 32-37, 39, and 44-50 be withdrawn.

Conclusion

The foregoing demonstrates that claims 1-41 and 43-53 are patentable. This application is therefore in condition for allowance. Reconsideration and allowance are accordingly respectfully requested.

Respectfully submitted,

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